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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/723,687	PATIL ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,12,13,15-18,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,12,13,15-18,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4-9, 12-13, 15-18, and 21-22 have been considered.

2. In view of the Appeal Brief filed on 08 June 2004, PROSECUTION IS HEREBY REOPENED. The additional rejection is set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the following two options:

   a. (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

   b. (2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

4. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1, 4-8, 18, and 21-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1 are 4-8 non-statutory since they are, in essence, claiming an instruction's functionality without having a tangible final result. The

claims simply recite that these type of instructions exist, but does not show how this affects the system. Simply having an instruction "to provide prediction information for a separate conditional branch instruction" does not constitute a tangible final result. There is no recitation of how this instruction would influence the system during execution, since the claim language is not concrete on the instruction's affects on the system, since all it does is "provide prediction information."

7. Claims 18 and 21-22 are non-statutory due to the conditional nature in its use of the branch prediction information. There is nothing in the claim stating what occurs when the decoded instruction is a not a branch prediction software instruction, so the final step recited in the claim would be decoding instructions. Decoding and fetching instructions are preliminary steps that occur in all systems, and, in this instance, the decoding step is equivalent to merely determining if something is true or not. Determining is not a tangible final result, since it does not affect the system in any form.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4-9, 12-13, 15-18, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mallick et al., U.S. Patent Number 5,752,014 (herein referred to as Mallick) in view of Intel's Intel® IA-64 Architecture Software Developer's Manual Volume 1: IA-64

Application Architecture (herein referred to as Intel Volume 1) and in further view of Blaner et al., U.S. Patent Number 5,649,178 (herein referred to as Blaner).

10. Referring to claim 1, Mallick has taught a computer system, comprising:

a. A processor which includes a hardware branch predictor (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; and Figure 1); and

b. A program of software instructions executed by said processor, said software instructions including conditional branch instructions (Mallick Abstract; column 1, lines 19-31 and 38-55; column 3, line 53 to column 55, line 24; and Figure 1)

11. Mallick has not taught separate static branch prediction instructions. Intel Volume 1 has taught separate static branch prediction instructions (Intel Volume 1 pages 4-29 to 4-31, Branch Prediction Hints). A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

12. In addition, Mallick has not taught a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction. Blaner has taught a plurality of groups of static branch prediction bits, each group being configurable to provide prediction information for a separate conditional branch instruction (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4). A person of ordinary skill in the art at the time the invention was made

would have recognized, and as taught by Blaner, that this improves branch prediction accuracy, thereby reducing the performance penalty caused by branch instruction execution and branch misprediction (Blaner column 1, line 48 to column 2, line 8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device of Blaner in the device of Mallick to improve branch prediction performance.

13. Referring to claim 9, Mallick has taught a processor, comprising:

a. Fetch logic that fetches program instructions from a source external to said processor (Mallick Abstract; column 3, line 53 to column 4, line 24; column 5, lines 1-12; and Figure 1);

b. A dynamic branch predictor coupled to said fetch logic, said dynamic branch predictor supplies predictions regarding conditional branch instructions to said fetch logic (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; and Figure 1);

c. An instruction queue coupled to said dynamic predictor, said fetch logic storing fetched instructions in said instruction queue (Mallick Abstract; column 3, line 53 to column 4, line 24); and

d. An execution unit coupled to said instruction queue and executing instructions provided from said instruction queue (Mallick Abstract column 1, lines 19-31 and 38-55; column 2, line 69 to column 3, line 2; and column 5, lines 25-42);

14. Mallick has not taught said fetch logic examines fetched instructions for a predetermined register identifier that identifies that instruction as a static branch prediction instruction. Intel Volume 1 has taught said fetch logic examines fetched instructions for a predetermined register

identifier that identifies that instruction (Intel Volume 1 page 4-29). In regards to Intel Volume 1, it must be determined whether a branch prediction instruction exists in order for the processor to chose whether to ignore the instruction or not and it does not matter whether the processor determines this in the fetch or not, because it functions the same. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

15. In addition, Mallick has not taught separate static branch prediction information about a plurality of conditional branch instructions. Blaner has taught separate static branch prediction information about a plurality of conditional branch instructions (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Blaner, that this improves branch prediction accuracy, thereby reducing the performance penalty caused by branch instruction execution and branch misprediction (Blaner column 1, line 48 to column 2, line 8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device of Blaner in the device of Mallick to improve branch prediction performance.

16. Referring to claims 4, 12, and 21, Mallick has not taught

a. Wherein each group of static branch prediction bits comprises a pair of bits (Applicant's claims 4 and 12);

b. Wherein said branch prediction information comprises pairs of bits, each pair corresponding to another instructions (Applicant's claim 21)

17. Blaner has taught

a. Wherein each group of static branch prediction bits comprises a pair of bits (Applicant's claims 4 and 12) (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4);

b. Wherein said branch prediction information comprises pairs of bits, each pair corresponding to another instructions (Applicant's claim 21) (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4).

18. In regards to Blaner, there are plural prediction bits (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Blaner, that this improves branch prediction accuracy, thereby reducing the performance penalty caused by branch instruction execution and branch misprediction (Blaner column 1, line 48 to column 2, line 8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device of Blaner in the device of Mallick to improve branch prediction performance.

19. Referring to claims 5-6, 13, and 22, Mallick has not taught:

a. Wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken (Applicant's claims 5, 13, and 22);

b. Wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken (Applicant's claims 6).

20. Intel Volume 1 has taught:

a. Wherein said prediction information includes a member selected from the group consisting of: do not use static prediction, predict taken, and predict not taken (Applicant's claim 5, 13, and 22) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions).

b. Wherein each pair of prediction bits corresponds to another instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static prediction, 10 means predict taken and 11 means predict not taken (Applicant's claims 6) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions). In regards to Intel Volume 1, the exact bit representations does not matter, because the functionality is the same. The exact bit representations are more of a design choice than inventive matter.

21. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

22. Referring to claims 7, 15, and 17 Mallick has not taught:

a. Wherein said static branch prediction bits comprises static branch prediction information that comprises encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor (Applicant's claims 7 and 15);

b. Wherein said predetermined identifier comprises a register identifier (Applicant's claim 17).

23. Intel Volume 1 has taught:

a. Wherein said static branch prediction bits comprises static branch prediction information that comprises encoded information directing the processor to ignore the predictions supplied by the hardware branch predictor (Applicant's claims 7 and 15) (Intel Volume 1 page 4-30 to page 4-31, Branch Prediction Instructions).

b. Wherein said predetermined identifier comprises a register identifier (Applicant's claim 17) (Intel Volume 1 page 4-29).

24. A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

25. Referring to claims 8 and 16, Mallick has taught wherein said hardware branch predictor comprises a log in which the results of all executed conditional branch instructions are stored (Mallick column 2, lines 10-15; column 6, lines 63-67; column 7, lines 36-54; Figure 2, element 68; and Figure 3).

26. Referring to claim 18, Mallick has taught a method of predicting the outcome of conditional branch instructions, comprising:

a. Including a static branch predictor software instruction in a program, said branch prediction software instruction (Intel Volume 1 pages 4-30 to 4-31, Branch Prediction Instructions);

b. Fetching said branch prediction software instructions (Mallick Abstract; column 3, line 53 to column 3, line 24; column 5, lines 1-12; and Figure 1);

c. Decoding said branch prediction software instructions to determine if said decoded instruction is a branch prediction software instruction (Mallick Abstract; column 1, lines 19-31 and 38-55; column 2, line 62 to column 3, line 9; column 3, line 53 to column 4, line 24; column 5, lines 13-24; and Figure 1).

27. Mallick has not taught if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction. Intel Volume 1 has taught if said decoded instruction is a branch prediction software instruction, then using said branch prediction information for branch prediction (Intel Volume 1 pages 4-30 to 4-31, Branch Prediction Instructions). A person of ordinary skill in the art at the time the invention was made would have recognized that the information about branch behavior provided by the branch prediction instruction improves branch prediction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the branch prediction instructions of Intel Volume 1 in the device of Mallick to improve branch prediction.

28. In addition, Mallick has not taught branch prediction information configurable to pertaining to a plurality of conditional branch instructions in the program. Blaner has taught

branch prediction information configurable to pertaining to a plurality of conditional branch instructions in the program (Blaner Abstract; column 2, lines 12-34 and 38-47; column 6, line 20 to column 7, line 18; and Figure 4). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by Blaner, that this improves branch prediction accuracy, thereby reducing the performance penalty caused by branch instruction execution and branch misprediction (Blaner column 1, line 48 to column 2, line 8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device of Blaner in the device of Mallick to improve branch prediction performance.

Response to Arguments

29. Applicant's arguments filed 10 June 2004 have been fully considered but they are not persuasive. The Appeal Brief argues in essence on pages 4-8

> ... At most, Intel Volume 1 discloses a branch prediction instruction that provides prediction information for only one branch conditional instruction...

30. This has not been found persuasive. The number of future branches the static branch prediction instruction predicts is not a patentable feature. Whether it is one branch or multiple branches does not matter. As Intel teaches, assuming Applicants' arguments are true, then multiple prediction branches contain the same information and affect the system the same as Applicants' single instruction. Simply adding a plurality of operand fields to an instruction is not a patentable feature if only because Applicants' would be claiming an instruction and the instruction's format, both of which are non-statutory subject matter.

31. Also, Applicant's arguments revolve around claim language that appears to more of an intended use of the instruction, which is non-limiting subject matter. The claim language being argued is describing an instruction that the system executes, i.e. uses, not the functionality of the system, processor, or method or the affects of the instruction's execution on the system. Therefore, the argued claim language is an intended use, which is non-limiting subject matter.

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J Li
Art Unit 2183
15 April 2007

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100